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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,880	04/06/2006	Shunpei Yamazaki	740756-2949	5429

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EXAMINER	
TAYLOR, EARL N	

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2818	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/574,880	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	EARL N. TAYLOR	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *10-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 7 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki (U.S. Patent 6,891,236 B1).

1. Referring to Claim 1, Yamazaki teaches, in Fig. 7, 8 and 21B, a light-emitting device comprising: a light-emitting element in which a light-emitting material (29) is sandwiched between a pair of electrodes (27 and 30) in a pixel; and a thin film transistor (23; Col. 26, Line 50; Fig. 8A and 8B) including, from a substrate (10 in Fig. 21B; 401 in Fig. 8B) side, a lamination of: a gate electrode (403); a gate insulating layer (402 and 404) formed in contact with the gate electrode (403), the gate insulating layer at least containing including at least a layer comprising a silicon nitride oxide (402) and a layer

comprising a silicon oxide (404); and a semiconductor layer (layer comprising elements 405, 406, 407, 409, 411, 413); wherein the light-emitting element and the thin film transistor (23) are connected in the pixel as shown in Fig. 21B (see Col. 26, Line 15 to Col. 28, Line 5).

The language, term, or phrase "a gate electrode formed by fusing conductive nanoparticles", is directed towards the process of forming a gate electrode. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the language only requires a gate electrode, which does not distinguish the invention from Yamazaki, who teaches the structure as claimed.

2. Referring to Claim 2, Yamazaki teaches, in Fig. 7, 8 and 21B, a light-emitting device comprising: a light-emitting element in which a light-emitting material (29) is

sandwiched between a pair of electrodes (27 and 30) in a pixel; and a thin film transistor (23; Col. 26, Line 50; Fig. 8A and 8B) including, from a substrate (10 in Fig. 21B; 401 in Fig. 8B) side, a lamination of: a gate electrode (403); a gate insulating layer (402 and 404) formed in contact with the gate electrode (403), the gate insulating layer at least containing including at least a layer comprising a silicon nitride oxide (402) and a layer comprising a silicon oxide (404); and a semiconductor layer (layer comprising elements 405, 406, 407, 409, 411, 413); wirings connected to a source and a drain as shown in Fig. 21B; and a silicon nitride oxide layer (interlayer insulating film 419 of Fig. 8B; like element interlayer insulating film 223 of Fig. 6C; Col. 13, Lines 28-40) formed by being in contact with the wirings; wherein the light-emitting element and the thin film transistor (23) are connected in the pixel as shown in Fig. 21B (see Col. 26, Line 15 to Col. 28, Line 5).

The language, term, or phrase "a gate electrode formed by fusing conductive nanoparticles" and "wirings connected to a source and a drain and formed by fusing conductive nanoparticles", is directed towards the process of forming a gate electrode and the wirings. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a

"product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the language only requires a gate electrode and wirings connected to a source and a drain, which does not distinguish the invention from Yamazaki, who teaches the structure as claimed.

3. Referring to Claim 3, Yamazaki teaches in Fig. 7, 8, 17 and 21B, a light-emitting device comprising: a light-emitting element in which a light-emitting material (29) is sandwiched between a pair of electrodes (27 and 30) in a pixel (details shown Fig. 21B); a first thin film transistor (23; Fig. 21B; details shown Fig. 8B) including, from a substrate side, a lamination of: a gate electrode (403); a gate insulating layer (402 and 404) formed in contact with the gate electrode (403), the gate insulating layer at least containing including at least a layer comprising a silicon nitride oxide (402) and a layer comprising a silicon oxide (404); and a semiconductor layer (layer comprising elements 405, 406, 407, 409, 411, 413); a driver circuit (22 of Fig. 21B; details shown in Fig. 7B; schematic connection shown as 1202 in Fig. 17) including a second thin film transistor formed by having the same layer structure as that of the first thin film transistor; and Fig. 17 (Col. 23, Lines 45-65) shows the schematic of connecting the first thin film transistor (1210; pixel switching transistor 23 of Fig. 21B) having a wiring (1230) extended from the driver circuit (1202) and connecting to the gate electrode of the first thin film

transistor (1210; 23 of Fig. 21B), wherein the light-emitting element and the thin film transistor are connected in the pixel as shown in Fig. 21B (see Col. 26, Line 15 to Col. 28, Line 5).

The language, term, or phrase "a gate electrode formed by fusing conductive nanoparticles" and "wirings connected to a source and a drain and formed by fusing conductive nanoparticles", is directed towards the process of forming a gate electrode and the wirings. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the language only requires a gate electrode and wirings connected to a source and a drain, which does not distinguish the invention from Yamazaki, who teaches the structure as claimed.

4. Referring to Claim 4, Yamazaki teaches in Fig. 7, 8, 17 and 21B, a light-emitting device comprising: a light-emitting element in which a light-emitting material (29) is sandwiched between a pair of electrodes (27 and 30) in a pixel (details shown Fig. 21B); a first thin film transistor (23; Fig. 21B; details shown Fig. 8B) including, from a substrate side, a lamination of: a gate electrode (403); a gate insulating layer (402 and 404) formed in contact with the gate electrode (403), the gate insulating layer at least containing including at least a layer comprising a silicon nitride oxide (402) and a layer comprising a silicon oxide (404); and a semiconductor layer (layer comprising elements 405, 406, 407, 409, 411, 413); wirings connected to a source and a drain as shown in Fig. 21B; and a silicon nitride oxide layer (interlayer insulating film 419 of Fig. 8B; like element interlayer insulating film 223 of Fig. 6C; Col. 13, Lines 28-40) formed by being in contact with the wirings; a driver circuit (22 of Fig. 21B; details shown in Fig. 7B; schematic connection shown as 1202 in Fig. 17) including a second thin film transistor formed by having the same layer structure as that of the first thin film transistor; and Fig. 17 (Col. 23, Lines 45-65) shows the schematic of connecting the first thin film transistor (1210; pixel switching transistor 23 of Fig. 21B) having a wiring (1230) extended from the driver circuit (1202) and connecting to the gate electrode of the first thin film transistor (1210; 23 of Fig. 21B), wherein the light-emitting element and the thin film transistor are connected in the pixel as shown in Fig. 21B (see Col. 26, Line 15 to Col. 28, Line 5)

5. Referring to Claim 7, Yamazaki further teaches wherein the driver circuit is composed only of an n-channel type thin film transistor (Fig. 7B).

6. Referring to Claim 9, Yamazaki further teaches wherein the light emitting device is a display screen (Fig. 18).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being obvious over Fujii et al. (U.S. Patent Application Publication 2005/0074963 A1) in view of Yu (U.S. Patent 6,323,143 B1)

7. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer

in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

8. Referring Claim 1, Fujii teaches in Fig. 18-19, a light-emitting device comprising: a light-emitting element (908) in which a light-emitting material (903) is sandwiched between a pair of electrodes (909 and 904) in a pixel; and a thin film transistor (6700) including, from a substrate side, a lamination of (par. 208 referencing TFTs formed by Embodiment Mode 1): a gate electrode (106) formed by fusing conductive nanoparticles (par. 43); a gate insulating layer (106) formed in contact with the gate electrode (106), at least containing a layer comprising a silicon nitride or silicon oxide (par. 52); and a semiconductor layer (107); wherein the light-emitting element and the thin film transistor are connected in the pixel (par. 208-212).

Fujii does not explicitly teach wherein the gate insulating layer (106) includes a layer comprising silicon nitride or silicon nitride oxide and a layer comprising silicon oxide.

Yu teaches a gate insulating layer comprising a silicon nitride layer (12) and a silicon oxide layer (14) (Col. 3, Line 51 to Col. 4, Line 51).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the gate insulating layer comprising a silicon nitride layer and a silicon oxide layer as taught by Yu in place of the gate insulating layer of Fujii in order to reduce leakage currents.

The language, term, or phrase "a gate electrode formed by fusing conductive nanoparticles", is directed towards the process of forming a gate electrode. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the language only requires a gate electrode, which does not distinguish the invention from Fujii in view of Yu, who teaches the structure as claimed.

9. Referring to Claim 2, Fujii teaches in Fig. 18-19, a light-emitting device comprising: a light-emitting element (908) in which a light-emitting material (903) is sandwiched between a pair of electrodes (909 and 904) in a pixel; and a thin film transistor (6700) including, from a substrate side, a lamination of (par. 208 referencing TFTs formed by Embodiment Mode 1): a gate electrode (106) formed by fusing conductive nanoparticles (par. 43); a gate insulating layer (106) formed in contact with

the gate electrode (106), at least containing a layer comprising a silicon nitride or silicon oxide layer (par. 52); and a semiconductor layer (107); wirings (115 and 116; par. 10 and 60) connected to a source and a drain and formed by fusing conductive nanoparticles; and a silicon nitride layer or silicon nitride oxide layer (118; par. 63) formed by being in contact with the wirings (115 and 116); wherein the light-emitting element and the thin film transistor are connected in the pixel (par. 208-212).

Fujii does not explicitly teach wherein the gate insulating layer (106) includes a layer comprising silicon nitride or silicon nitride oxide and a layer comprising silicon oxide.

Yu teaches a gate insulating layer comprising a silicon nitride layer (12) and a silicon oxide layer (14) (Col. 3, Line 51 to Col. 4, Line 51).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the gate insulating layer comprising a silicon nitride layer and a silicon oxide layer as taught by Yu in place of the gate insulating layer of Fujii in order to reduce leakage currents.

The language, term, or phrase "a gate electrode formed by fusing conductive nanoparticles" and "wirings ... formed by fusing conductive nanoparticles", is directed towards the process of forming a gate electrode. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal

with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the language only requires a gate electrode and wirings, which does not distinguish the invention from Fujii in view of Yu, who teaches the structure as claimed.

10. Referring to Claim 3, Fujii teaches in Fig. 18-19, a light-emitting device comprising: a light-emitting element (908) in which a light-emitting material (903) is sandwiched between a pair of electrodes (909 and 904) in a pixel; and a thin film transistor (6700) including, from a substrate side, a lamination of (par. 208 referencing TFTs formed by Embodiment Mode 1): a gate electrode (106) formed by fusing conductive nanoparticles (par. 43); a gate insulating layer (106) formed in contact with the gate electrode (106), at least containing a layer comprising a silicon nitride (par. 52); and a semiconductor layer (107); a driver circuit including a second thin film transistor (6701) formed by having the same layer structure as that of the first thin film transistor (6700) (par. 208 and 209); and a wiring (shown in Fig. 18A, 18B and 19A) extended from the driver circuit and connecting to the gate electrode (6700) of the first thin film transistor (6700); wherein the light-emitting element and the thin film transistor are connected in the pixel (par. 208-212).

Fujii does not explicitly teach wherein the gate insulating layer (106) includes a layer comprising silicon nitride or silicon nitride oxide and a layer comprising silicon oxide.

Yu teaches a gate insulating layer comprising a silicon nitride layer (12) and a silicon oxide layer (14) (Col. 3, Line 51 to Col. 4, Line 51).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the gate insulating layer comprising a silicon nitride layer and a silicon oxide layer as taught by Yu in place of the gate insulating layer of Fujii in order to reduce leakage currents.

The language, term, or phrase "a gate electrode formed by fusing conductive nanoparticles", is directed towards the process of forming a gate electrode. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that

applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the language only requires a gate electrode, which does not distinguish the invention from Fujii in view of Yu, who teaches the structure as claimed.

11. Referring to Claim 4, Fujii teaches in Fig. 18-19, a light-emitting device comprising: a light-emitting element (908) in which a light-emitting material (903) is sandwiched between a pair of electrodes (909 and 904) in a pixel; and a thin film transistor (6700) including, from a substrate side, a lamination of (par. 208 referencing TFTs formed by Embodiment Mode 1): a gate electrode (106) formed by fusing conductive nanoparticles (par. 43); a gate insulating layer (106) formed in contact with the gate electrode (106), at least containing a layer comprising a silicon nitride (par. 52); and a semiconductor layer (107); wirings (115 and 116; par. 10 and 60) connected to a source and a drain and formed by fusing conductive nanoparticles; and a silicon nitride layer or silicon nitride oxide layer (118; par. 63) formed by being in contact with the wirings (115 and 116); a driver circuit including a second thin film transistor (6701) formed by having the same layer structure as that of the first thin film transistor (6700) (par. 208 and 209); and a wiring (shown in Fig. 18A, 18B and 19A) extended from the driver circuit and connecting to the gate electrode (6700) of the first thin film transistor (6700); wherein the light-emitting element and the thin film transistor are connected in the pixel (par. 208-212).

Fujii does not explicitly teach wherein the gate insulating layer (106) includes a layer comprising silicon nitride or silicon nitride oxide and a layer comprising silicon oxide.

Yu teaches a gate insulating layer comprising a silicon nitride layer (12) and a silicon oxide layer (14) (Col. 3, Line 51 to Col. 4, Line 51).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the gate insulating layer comprising a silicon nitride layer and a silicon oxide layer as taught by Yu in place of the gate insulating layer of Fujii in order to reduce leakage currents.

The language, term, or phrase "a gate electrode formed by fusing conductive nanoparticles" and "wirings ... formed by fusing conductive nanoparticles", is directed towards the process of forming a gate electrode. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, *per se*, no matter how actually made. *In re Hirao,* 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise.

The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

As such, the language only requires a gate electrode and wirings, which does not distinguish the invention from Fujii in view of Yu, who teaches the structure as claimed.

12. Referring to Claim 5, Fujii further teaches wherein the conductive nanoparticles comprise silver (par. 15, 43, 87 and 110).

13. Referring to Claim 6, Fujii further teaches wherein the semiconductor layer contains hydrogen and halogen and is a semi-amorphous semiconductor having a crystal structure (par. 53, 149 and167).

14. Referring to Claim 7, Fujii further teaches wherein the driver circuit is composed only of an n-channel type thin film transistor (par. 57; the TFT can be either P-type or N-type exclusively).

15. Referring to Claim 8, Fujii further teaches wherein the thin film transistor includes the semiconductor layer containing hydrogen and halogen and which is a semiconductor having a crystal structure (par. 53, 149 and167), thus because Fujii teaches all of the claimed structural elements, the thin film transistor is capable of being operated in electric field effect mobility of from 1 $cm^2/V\cdot$ sec to 15 $cm^2/V\cdot$ sec cm^2. See also paragraph 150 wherein the TFT mobility is 1 $cm^2/V\cdot$ sec to 10 $cm^2/V\cdot$ sec cm^2.

16. Referring to Claim 9, Fujii further teaches wherein the light-emitting device is a display screen (par. 226; Fig. 16-16C).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Telephone / Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl N. Taylor whose telephone number is (571) 272-8894. The examiner can normally be reached on Monday-Friday from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Earl N. Taylor

/DAVID VU/
Primary Examiner, Art Unit 2818